	L #	Hits	Search Text	DBs
1	L1	1160	(cache near5 coheren$3) and (shared adj1 memory) and (((multi multiple) adj1 processor) multiprocessor)	USPAT; US-PGPUB
2	L2	48	((cache near5 coheren$3) and (shared adj1 memory) and (((multi multiple) adj1 processor) multiprocessor)).ab,ti.	USPAT; US-PGPUB
3	L4	4	2 and 3	USPAT; US-PGPUB
4	L3	62	cache near10 line near10 lock$3 and 1	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040059877 A1	☐	Method and apparatus for implementing cache state as history of read/write shared data	711/144
2	US 20040054855 A1	☒	Shared memory multiprocessor performing cache coherence control and node controller therefor	711/147
3	US 20040034747 A1	☒	Scalable cache coherent distributed shared memory processing system	711/148
4	US 20030163543 A1	☒	Method and system for cache coherence in DSM multiprocessor system without growth of the sharing vector	709/214
5	US 20030115402 A1	☒	Multiprocessor system	711/1
6	US 20020166032 A1	☒	Method for verifying abstract memory models of shared memory multiprocessors	711/141
7	US 20020144063 A1	☒	Multiprocessor cache coherence management	711/141
8	US 20020138698 A1	☒	System and method for caching directory information in a shared memory multiprocessor system	711/130
9	US 20020133674 A1	☒	Bandwidth-adaptive, hybrid, cache-coherence protocol	711/141
10	US 20020129208 A1	☒	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
11	US 20020100020 A1	☒	Method for maintaining cache coherency in software in a shared memory system	717/124
12	US 20020100019 A1	☒	Software shared memory bus	717/124
13	US 20020073071 A1	☒	Transactional memory for distributed shared memory multi-processor computer systems	707/1
14	US 20020053004 A1	☒	ASYNCHRONOUS CACHE COHERENCE ARCHITECTURE IN A SHARED MEMORY MULTIPROCESSOR WITH POINT-TO-POINT LINKS	711/119
15	US 20020052914 A1	☒	SOFTWARE PARTITIONED MULTI-PROCESSOR SYSTEM WITH FLEXIBLE RESOURCE SHARING LEVELS	709/203
16	US 20010052054 A1	☒	APPARATUS AND METHOD FOR PARTITIONED MEMORY PROTECTION IN CACHE COHERENT SYMMETRIC MULTIPROCESSOR SYSTEMS	711/147
17	US 20010005873 A1	☒	Shared memory multiprocessor performing cache coherence control and node controller therefor	710/305

	Document ID	U	Title	Current OR
18	US 6711662 B2	☒	Multiprocessor cache coherence management	711/204
19	US 6675262 B1	☒	Multi-processor computer system with cache-flushing system using memory recall	711/135
20	US 6636949 B2	☒	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
21	US 6636926 B2	☒	Shared memory multiprocessor performing cache coherence control and node controller therefor	710/305
22	US 6633945 B1	☒	Fully connected cache coherent multiprocessing systems	710/316
23	US 6546471 B1	☒	Shared memory multiprocessor performing cache coherency	711/148
24	US 6542926 B2	☒	Software partitioned multi-processor system with flexible resource sharing levels	709/213
25	US 6526481 B1	☒	Adaptive cache coherence protocols	711/147
26	US 6516442 B1	☒	Channel interface and protocols for cache coherency in a scalable symmetric multiprocessor system	714/776
27	US 6510496 B1	☒	Shared memory multiprocessor system and method with address translation between partitions and resetting of nodes included in other partitions	711/147
28	US 6457100 B1	☒	Scaleable shared-memory multi-processor computer system having repetitive chip structure with efficient busing and coherence controls	711/119
29	US 6449699 B2	☒	Apparatus and method for partitioned memory protection in cache coherent symmetric multiprocessor systems	711/147
30	US 6360231 B1	☒	Transactional memory for distributed shared memory multi-processor computer systems	707/201
31	US 6356983 B1	☒	System and method providing cache coherency and atomic memory operations in a multiprocessor computer architecture	711/145
32	US 6341337 B1	☒	Apparatus and method for implementing a snoop bus protocol without snoop-in and snoop-out logic	711/146
33	US 6209064 B1	☒	Cache coherence unit with integrated message passing and memory protection for a distributed, shared memory multiprocessor system	711/141
34	US 6148375 A	☒	Hierarchical bus simple COMA architecture for shared memory multiprocessors having a bus directly interconnecting caches between nodes	711/130
35	US 6088770 A	☒	Shared memory multiprocessor performing cache coherency	711/148
36	US 6088768 A	☒	Method and system for maintaining cache coherence in a multiprocessor-multicache environment having unordered communication	711/141
37	US 5895486 A	☒	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121
38	US 5835950 A	☒	Self-invalidation method for reducing coherence overheads in a bus-based shared-memory multiprocessor apparatus	711/144
39	US 5822763 A	☒	Cache coherence protocol for reducing the effects of false sharing in non-bus-based shared-memory multiprocessors	711/141
40	US 5809536 A	☒	Method for reducing the number of coherency cycles within a directory-based cache coherency memory system uitilizing a memory state cache	711/144

	Document ID	U	Title	Current OR
41	US 5802582 A	☒	Explicit coherence using split-phase controls	711/152
42	US 5752258 A	☒	Encoding method for directory state in cache coherent distributed shared memory system	711/120
43	US 5737757 A	☒	Cache tag system for use with multiple processors including the most recently requested processor identification	711/145
44	US 5715428 A	☒	Apparatus for maintaining multilevel cache hierarchy coherency in a multiprocessor computer system	711/141
45	US 5511226 A	☒	System for generating snoop addresses and conditionally generating source addresses whenever there is no snoop hit, the source addresses lagging behind the corresponding snoop addresses	711/146
46	US 5404483 A	☒	Processor and method for delaying the processing of cache coherency transactions during outstanding cache fills	711/144
47	US 5276828 A	☒	Methods of maintaining cache coherence and processor synchronization in a multiprocessor system using send and receive instructions	709/248
48	US 5274787 A	☐	Method of copy-back cache coherence control and tightly coupled multi-processor system with split transfer system bus	711/143

	Document ID	U	Title	Current OR
1	US 20040059893 A1	☐	System and method to automatically stack and unstack java local variables	712/208
2	US 20030225979 A1	☒	Methods and apparatus for speculative probing of a remote cluster	711/141
3	US 20030225978 A1	☒	Methods and apparatus for speculative probing of a remote cluster	711/141
4	US 20030212741 A1	☒	Methods and apparatus for responding to a request cluster	709/203
5	US 20030210655 A1	☒	Methods and apparatus for responding to a request cluster	370/244
6	US 20030182514 A1	☒	Methods and apparatus for speculative probing with early completion and delayed request	711/141
7	US 20030182509 A1	☒	Methods and apparatus for speculative probing at a request cluster	711/119
8	US 20030182508 A1	☒	Methods and apparatus for speculative probing with early completion and early request	711/118
9	US 20030163642 A1	☒	Shared cache line update mechanism	711/121
10	US 20030065894 A1	☒	Technique for implementing a distributed lock in a processor-based device	711/152
11	US 20030046495 A1	☒	Streamlined cache coherency protocol system and method for a multiple processor single chip device	711/141
12	US 20030023794 A1	☒	Cache coherent split transaction memory bus architecture and protocol for a multi processor chip device	710/105
13	US 20020174305 A1	☒	Method and apparatus for controlling memory storage locks based on cache line ownership	711/145
14	US 20020147872 A1	☒	Sequentially performed compound compare-and-swap	710/200
15	US 20010052053 A1	☒	Stream processing unit for a multi-streaming processor	711/138
16	US 6944711 B2	☒	Technique for implementing a distributed lock in a processor-based device	711/152
17	US 6675262 B1	☒	Multi-processor computer system with cache-flushing system using memory recall	711/135
18	US 6625698 B2	☒	Method and apparatus for controlling memory storage locks based on cache line ownership	711/141

	Document ID	U	Title	Current OR
19	US 6493809 B1	☒	Maintaining order of write operations in a multiprocessor for memory consistency	711/167
20	US 6480918 B1	☒	Lingering locks with fairness control for multi-node computer systems	710/200
21	US 6473819 B1	☒	Scalable interruptible queue locks for shared-memory multiprocessor	710/200
22	US 6460124 B1	☒	Method of using delays to speed processing of inferred critical program portions	711/163
23	US 6460122 B1	☒	System, apparatus and method for multi-level cache in a multi-processor/multi-controller environment	711/154
24	US 6457100 B1	☒	Scaleable shared-memory multi-processor computer system having repetitive chip structure with efficient busing and coherence controls	711/119
25	US 6457087 B1	☒	Apparatus and method for a cache coherent shared memory multiprocessing system	710/305
26	US 6389515 B1	☒	System and method for avoiding deadlocks utilizing split lock operations to provide exclusive access to memory during non-atomic operations	711/141
27	US 6374329 B1	☒	High-availability super server	711/141
28	US 6356983 B1	☒	System and method providing cache coherency and atomic memory operations in a multiprocessor computer architecture	711/145
29	US 6226714 B1	☒	Method for invalidating cache lines on a sharing list	711/119
30	US 6141734 A	☒	Method and apparatus for optimizing the performance of LDxL and STxC interlock instructions in the context of a write invalidate protocol	711/144
31	US 6094709 A	☒	Cache coherence for lazy entry consistency in lockup-free caches	711/141
32	US 6092156 A	☒	System and method for avoiding deadlocks utilizing split lock operations to provide exclusive access to memory during non-atomic operations	711/145
33	US 6065077 A	☒	Apparatus and method for a cache coherent shared memory multiprocessing system	710/100
34	US 6041376 A	☒	Distributed shared memory system having a first node that prevents other nodes from accessing requested data until a processor on the first node controls the requested data	710/108
35	US 6026461 A	☒	Bus arbitration system for multiprocessor architecture	710/244
36	US 6006299 A	☒	Apparatus and method for caching lock conditions in a multi-processor system	710/108
37	US 6000007 A	☒	Caching in a multi-processor computer system	711/105
38	US 5987549 A	☒	Method and apparatus providing short latency round-robin arbitration for access to a shared resource	710/107
39	US 5983326 A	☒	Multiprocessing system including an enhanced blocking mechanism for read-to-share-transactions in a NUMA mode	711/147
40	US 5978874 A	☒	Implementing snooping on a split-transaction computer system bus	710/107
41	US 5960179 A	☒	Method and apparatus extending coherence domain beyond a computer system bus	710/107

	Document ID	U	Title	Current OR
42	US 5911052 A	☒	Split transaction snooping bus protocol	710/113
43	US 5900020 A	☒	Method and apparatus for maintaining an order of write operations by processors in a multiprocessor computer to maintain memory consistency	711/167
44	US 5893151 A	☒	Method and apparatus for maintaining cache coherency in a computer system with a highly pipelined bus and multiple conflicting snoop requests	711/140
45	US 5890200 A	☒	Method and apparatus for maintaining cache coherency in a computer system with a highly pipelined bus and multiple conflicting snoop requests	711/108
46	US 5887146 A	☒	Symmetric multiprocessing computer with non-uniform memory access architecture	710/104
47	US 5875464 A	☒	Computer system with private and shared partitions in cache	711/129
48	US 5864657 A	☒	Main memory system and checkpointing protocol for fault-tolerant computer system	714/15
49	US 5860159 A	☒	Multiprocessing system including an apparatus for optimizing spin--lock operations	711/151
50	US 5829033 A	☒	Optimizing responses in a coherent distributed electronic system including a computer system	711/141
51	US 5822763 A	☒	Cache coherence protocol for reducing the effects of false sharing in non-bus-based shared-memory multiprocessors	711/141
52	US 5802578 A	☒	Multinode computer system with cache for combined tags	711/147
53	US 5796939 A	☒	High frequency sampling of processor performance counters	714/47
54	US 5787267 A	☒	Caching method and circuit for a memory system with circuit module architecture	711/105
55	US 5784722 A	☒	Data processing system memory controller that selectively caches data associated with write requests	711/117
56	US 5751939 A	☒	Main memory system and checkpointing protocol for fault-tolerant computer system using an exclusive-or memory	714/15
57	US 5745672 A	☒	Main memory system and checkpointing protocol for a fault-tolerant computer system using a read buffer	714/6
58	US 5737514 A	☒	Remote checkpoint memory system and protocol for fault-tolerant computer system	714/13
59	US 5678026 A	☒	Multi-processor data processing system with control for granting multiple storage locks in parallel and parallel lock priority and second level cache priority queues	711/152
60	US 5574922 A	☒	Processor with sequences of processor instructions for locked memory updates	712/220
61	US 5230070 A	☒	Access authorization table for multi-processor caches	711/145
62	US 4775955 A	☒	Cache coherence mechanism based on locking	711/145